# SAC3118

GaAs MMIC Power Amplifier
27.5GHz～32GHz 35.5dBm

Rev2.1

## Features

- Frequency: 27.5GHz～32GHz
- Gain: 27dB
- Output $P_{-1}$dB: 35.5dBm
- Supply Voltage: +6V
- Power-Added Efficiency: 18%
- Die Size: 3.55mm×3.8mm×0.1mm
- Packaged: Bare Die

## Typical Applications

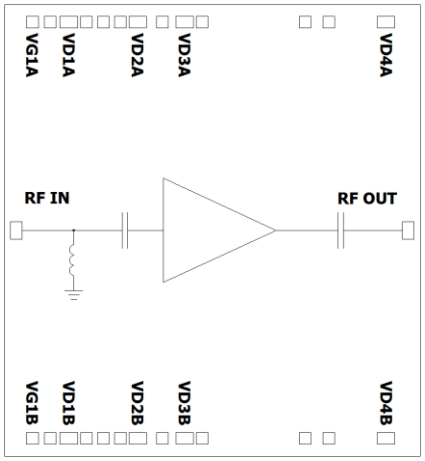
- Microwave radio including point to point communication
- Telecommunication
- Weather radar
- Optical communication
- Test instrumentation
- SatCom
- VSAT
- Military and Aerospce

## General Description

The SAC3118 is a Ka-band GaAs MMIC power amplifier. The SAC3118 provides 27 dB of gain, and 35.5dBm of output power for 1 dB compression and 18%PAE from a +6V supply.

The chip has surface passivation for protection and backside via holes and gold metallization to allow a conductive epoxy die attach process. This device is well suited for communications, Point to Point radio and radar applications.

## Functional Diagram




## Electrical Performance

$T_A$=25℃,$V_D$=+6V,$I_D$=2A,$Z_0$=50Ω, CW

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Frequency Range | | 27.5～32 | | GHz |
| Small Signal Gain | 23 | 27 | — | dB |
| Small Signal Gain Flatness | — | ±2 | — | dB |
| Reverse Isolation | — | -55 | — | dB |
| Input Return Loss | — | -10 | — | dB |
| Power-Added Efficiency | — | 18 | — | % |
| Output Power for 1 dB Compression ($OP_{-1}$dB) | 35 | 35.5 | — | dBm |
| Output Third Order Intercept($OIP_3$)* | — | 39 | — | dBm |
| Drain Voltage($V_D$) | — | 6 | 6.3 | V |
| Gate Current($I_G$) | — | 5 | 28 | mA |
| Supply Current($I_D$) | — | 3.2 | 3.7 | A |
| Thermal Resistance | — | 4.1 | — | ℃/W |

* Measurement taken at Pout / Tone = 18 dBm, fc= 30GHz,Δ f=10MHz

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## Absolute Maximum Ratings

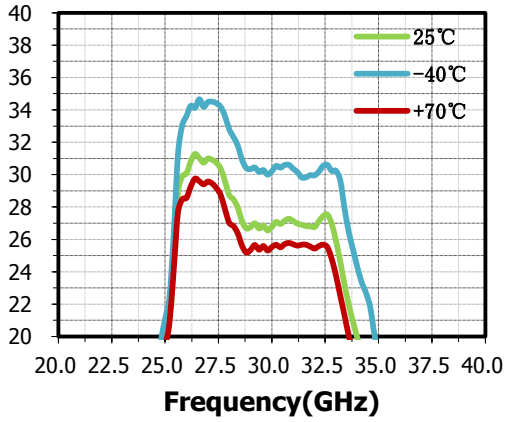
| | | | |
|---|---|---|---|
| Maximum Input Power | +14dBm | Operating Temperature | -40℃～+70℃ |
| Channel Temperature | +150℃ | Storage Temperature | -65℃～+150℃ |
| Maximum $V_D$ | +6.5V | Maximum $V_G$ | -1.2V |

## Typical Small Signal Performance Curve

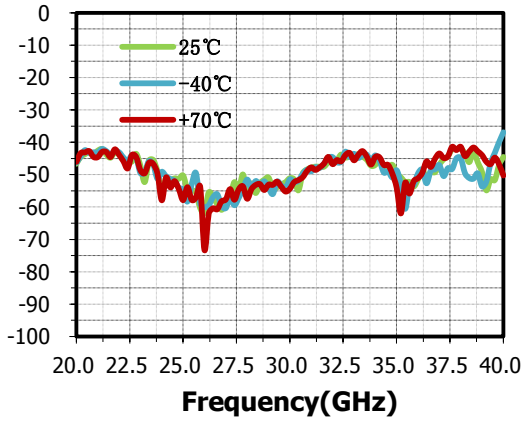
The results captured in the test-jig environment within connector plan

**$V_D$=+6v $I_D$=2A CW**

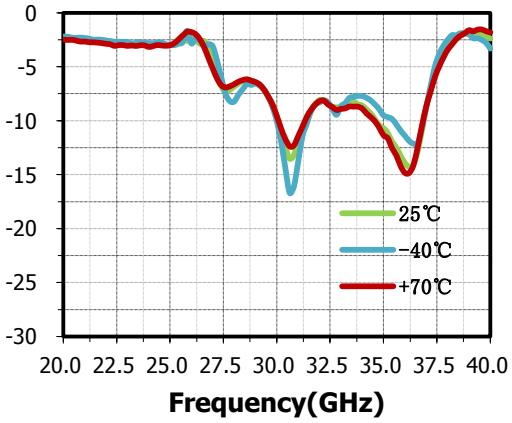
**Small Signal Gain(dB) vs.Temperature**



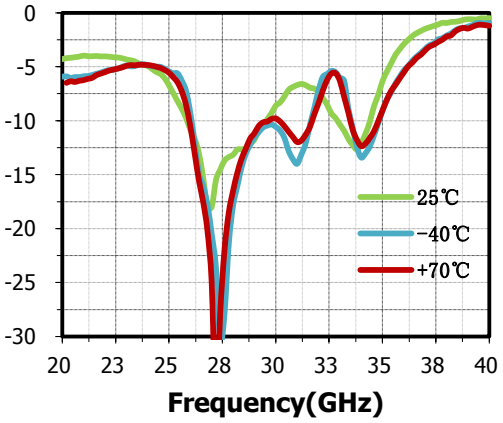

**Reverse Isolation(dB) vs.Temperature**




**Input Return Loss(dB) vs.Temperature**



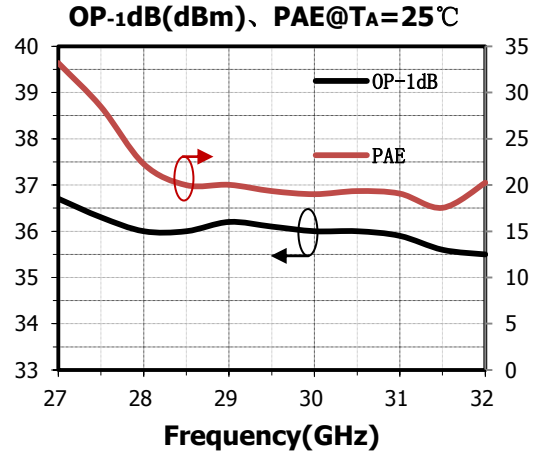

**Output Return Loss(dB) vs.Temperature**

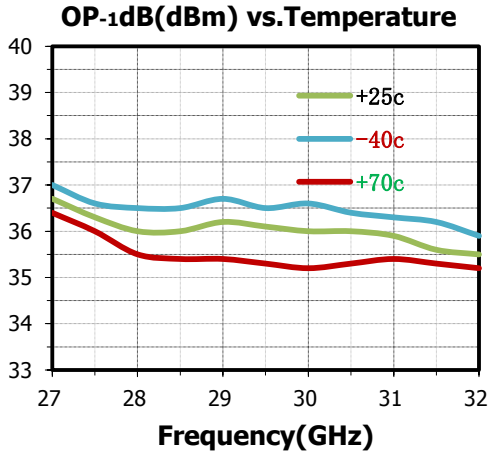


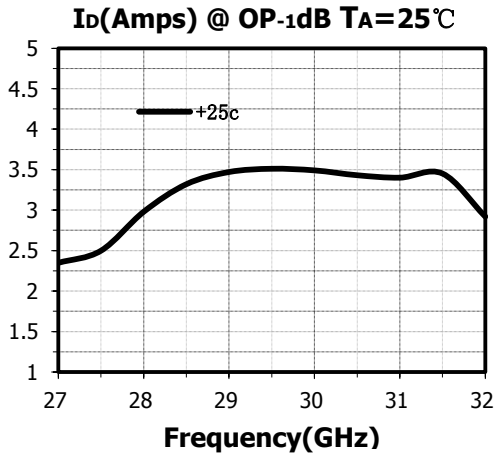
## Power and PAE Performance Curve

The results captured in the test-jig environment within connector plan, then de-embedded the housing an come back in the die plan

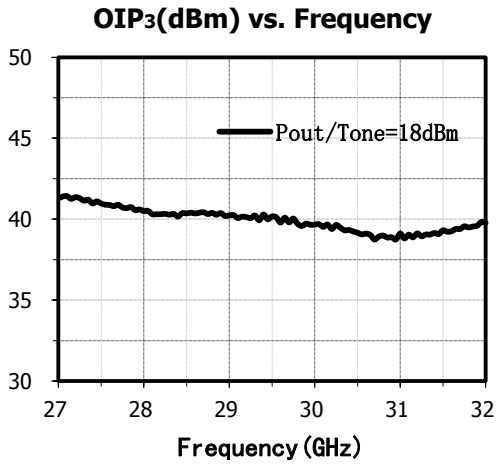
**$V_D$=+6V $I_D$=2A CW**

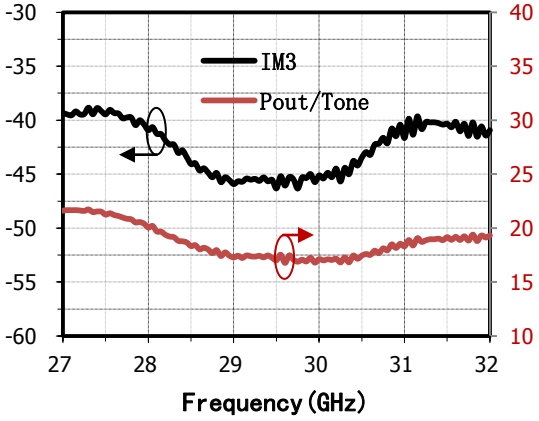



## $OIP_3$ 、IM3 Performance Curve

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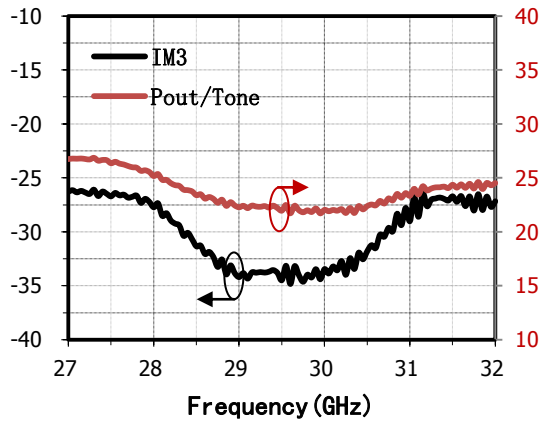
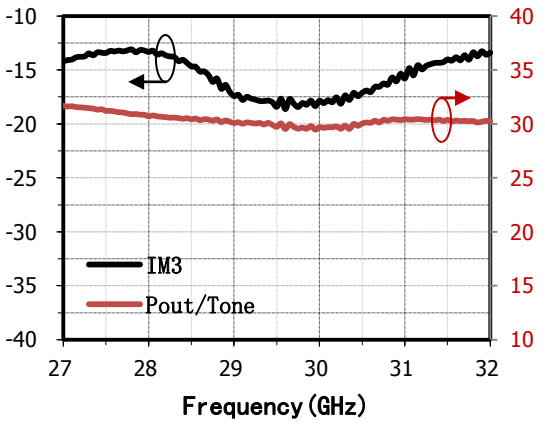
**IM3(dBc) vs. Pout(dBm) II**

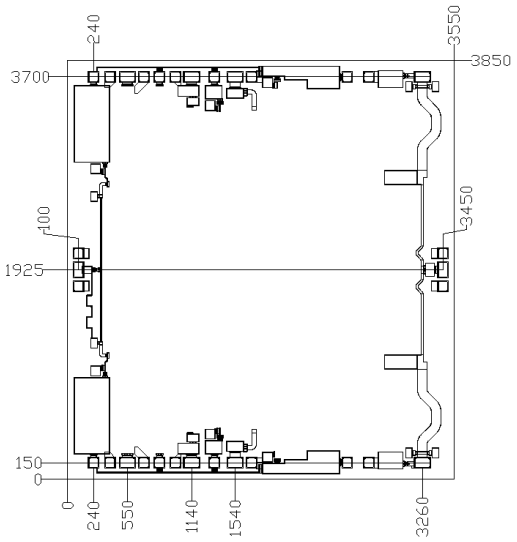



**IM3(dBc) vs. Pout(dBm) III**

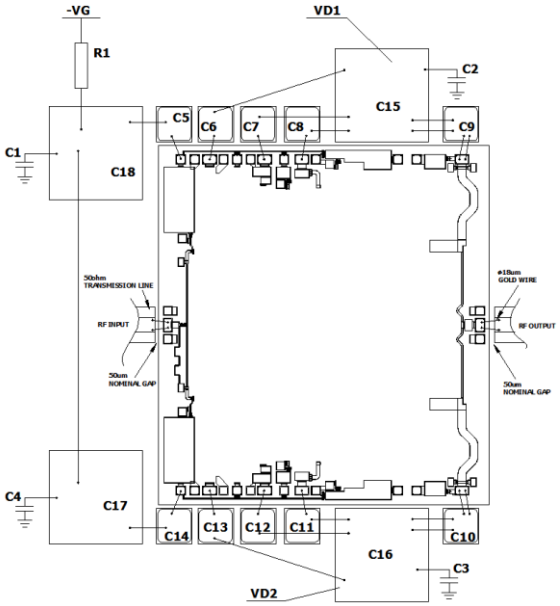



## Die Outline

**(all dimensions in μm)**




## Assembly Diagram




**Bonding pad size:**

150x100um VD1A～VD4A、VD1B～VD4B、RF IN、RFOUT pads

100x100um VG1A、VG1B pads

## Components List

| Reference Des. | Value | Part Number | Manuf. | Size |
|---|---|---|---|---|
| C1～C4 | 2.2uF | GRM155R61A225KE15D | Murata | 0402 |
| C5～C14 | 300pF | — | ANY | SLC |
| C15～C18 | 1000pF | — | ANY | SLC |
| R1* | 20Ω | — | ANY | 0603 |

* The value of R1 varies with the internal resistance of the gate bias circuit. When the internal resistance value of the gate bias circuit is less than 2Ω, R1=10 to 20 ohm is suitable.

### Notes

1. The SAC3118 is biased with a positive drain supply and negative gate supply.The recommended gate voltage is set to -0.7～-0.9 V.
2. RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 0.8 mil thermosonic wedge bonding is highly recommended as the loop height will be minimized. The RF input and output require a double bond wire as shown.
3. The backside of the SAC3118 is RF ground. Eutectic mounting is preferred, If using conductive epoxy, recommended epoxies is UNIMEC H9890-6A cured per the manufacturer's cure schedule. Epoxy should be applied in accordance with the manufacturers specifications and should avoid contact with the top surface of the die. An epoxy fillet should be visible around the total die periphery.
4. Bypass caps C1～C4 should be placed no farther than 1.5mm from the amplifier.

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